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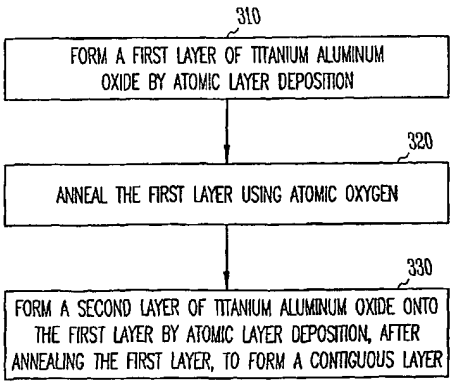
(54) Title: ATOMIC LAYER DEPOSITED TITANIUM ALUMINUM OXIDE FILMS



(57) Abstract: A dielectric layer containing an atomic layer deposited insulating metal oxide film having multiple metal components and a method of fabricating such a dielectric layer produce a reliable dielectric layer for use in a variety of electronic devices. Embodiments include conducting a number of annealing processes between a number of atomic layer deposition cycles for forming the metal oxide film. In an embodiment, a titanium aluminum oxide film is formed by depositing titanium and/or aluminum by atomic layer deposition onto a substrate surface. The deposited titanium and/or aluminum is annealed using atomic oxygen. After annealing, a layer of titanium aluminum oxide is formed on the annealed layer to form a contiguous layer of titanium aluminum oxide. Embodiments include structures for capacitors, transistors, memory devices, and electronic systems with dielectric layers containing an atomic layer deposited titanium aluminum oxide film, and methods for forming such structures.

WO 2006/026716 A1

ATOMIC LAYER DEPOSITED TITANIUM ALUMINUM OXIDE FILMS

Technical Field

This application relates generally to semiconductor devices and device fabrication and, more particularly, to dielectric layers and their method of fabrication.

Background

The semiconductor device industry has a market driven need to reduce the size of devices such as transistors. To reduce transistor size, the thickness of the silicon dioxide, SiO_2, gate dielectric is reduced in proportion to the shrinkage of the gate length. For example, a metal-oxide-semiconductor field effect transistor (MOSFET) would use a 1.5 nm thick SiO_2 gate dielectric for a gate length of 70 nm. A goal is to fabricate increasingly smaller and more reliable integrated circuits (ICs) for use in products such as processor chips, mobile telephones, and memory devices such as dynamic random access memories (DRAMs).

Currently, the semiconductor industry relies on the ability to reduce or scale the dimensions of its basic devices, primarily, the silicon based MOSFET. This device scaling includes scaling the gate dielectric, which has primarily been fabricated using silicon dioxide. A thermally grown amorphous SiO_2 layer provides an electrically and thermodynamically stable material, where the interface of the SiO_2 layer with underlying silicon provides a high quality interface as well as superior electrical isolation properties. However, increased scaling and other requirements in microelectronic devices have created the need to use other dielectric materials as gate dielectrics.

Summary

The abovementioned problems are addressed by the present invention and will be understood by reading and studying the following specification. An embodiment for a method for forming an electronic device includes forming a dielectric layer containing an insulating metal oxide film, in which the metal

oxide includes multiple metal components formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. In an embodiment, titanium and/or aluminum is deposited in an integrated circuit on a surface of a substrate by atomic layer deposition. The deposited material is annealed using atomic oxygen. After annealing, a layer of titanium aluminum oxide is formed on the annealed material by atomic layer deposition such that a contiguous layer of titanium aluminum oxide is formed. Embodiments include structures for capacitors, transistors, memory devices, and electronic systems with dielectric layers containing an atomic layer deposited titanium aluminum oxide film, and methods for forming such structures. These and other aspects, embodiments, advantages, and features will become apparent from the following description and the referenced drawings.

Brief Description of the Drawings

Figure 1 depicts an atomic layer deposition system for fabricating a dielectric layer containing a titanium aluminum oxide, according to various embodiments of the present invention.

Figure 2 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film using atomic layer deposition, according to various embodiments of the present invention.

Figure 3 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film using atomic layer deposition, according to the present invention.

Figure 4 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film using atomic layer deposition, according to the present invention.

Figure 5 shows an embodiment of a configuration of a transistor having a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Figure 6 shows an embodiment of a configuration of a floating gate transistor having a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Figure 7 shows an embodiment of a configuration of a capacitor having a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Figure 8 depicts an embodiment of a dielectric layer including a nanolaminate having at least one layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Figure 9 is a simplified diagram for an embodiment of a controller coupled to an electronic device having a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Figure 10 illustrates a diagram for an embodiment of an electronic system having devices with a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles, according to the present invention.

Detailed Description

The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present

invention. The various embodiments disclosed herein are not necessarily mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC) structure. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to generally include n-type and p-type semiconductors and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors or as semiconductors.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

A gate dielectric in a transistor has both a physical gate dielectric thickness and an equivalent oxide thickness (t_{eq}). The equivalent oxide thickness quantifies the electrical properties, such as capacitance, of the gate dielectric in terms of a representative physical thickness. t_{eq} is defined as the thickness of a theoretical SiO_2 layer that would be required to have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations.

A SiO_2 layer of thickness, t, deposited on a Si surface as a gate dielectric will have a t_{eq} larger than its thickness, t. This t_{eq} results from the capacitance in the surface channel on which the SiO_2 is deposited due to the formation of a depletion/inversion region. This depletion/inversion region can result in t_{eq} being from 3 to 6 Angstroms (Å) larger than the SiO_2 thickness, t. Thus, with the semiconductor industry driving to someday scale the gate dielectric equivalent oxide thickness to under 10 Å, the physical thickness for a SiO_2 layer used for a gate dielectric would be need to be approximately 4 to 7 Å.

Additional requirements on a SiO_2 layer would depend on the gate electrode used in conjunction with the SiO_2 gate dielectric. Using a conventional polysilicon gate would result in an additional increase in t_{eq} for the SiO_2 layer. This additional thickness could be eliminated by using a metal gate electrode, though metal gates are not currently used in typical complementary metal-oxide-semiconductor field effect transistor (CMOS) technology. Thus, future devices would be designed towards a physical SiO_2 gate dielectric layer of about 5 Å or less. Such a small thickness for a SiO_2 oxide layer creates additional problems.

Silicon dioxide is used as a gate dielectric, in part, due to its electrical isolation properties in a SiO_2 - Si based structure. This electrical isolation is due to the relatively large band gap of SiO_2 (8.9 eV) making it a good insulator from electrical conduction. Signification reductions in its band gap would eliminate it as a material for a gate dielectric. As the thickness of a SiO_2 layer decreases, the number of atomic layers, or monolayers of the material in the thickness decreases. At a certain thickness, the number of monolayers will be sufficiently small that the SiO_2 layer will not have a complete arrangement of atoms as in a larger or bulk layer. As a result of incomplete formation relative to a bulk structure, a thin SiO_2 layer of only one or two monolayers will not form a full band gap. The lack of a full band gap in a SiO_2 gate dielectric would cause an effective short between an underlying Si channel and an overlying polysilicon gate. This undesirable property sets a limit on the physical thickness to which a SiO_2 layer can be scaled. The minimum thickness due to this monolayer effect is thought to be about 7-8 Å. Therefore, for future devices to have a t_{eq} less than about 10 Å, other dielectrics than SiO_2 need to be considered for use as a gate dielectric.

For a typical dielectric layer used as a gate dielectric, the capacitance is determined as one for a parallel plate capacitance: $C = \kappa\epsilon_0 A/t$, where κ is the dielectric constant, ϵ_0 is the permittivity of free space, A is the area of the capacitor, and t is the thickness of the dielectric. The thickness, t, of a material is related to its t_{eq} for a given capacitance, with SiO_2 having a dielectric constant $\kappa_{ox} = 3.9$, as

$$t = (\kappa/\kappa_{ox}) t_{eq} = (\kappa/3.9) t_{eq}.$$

Thus, materials with a dielectric constant greater than that of SiO_2, 3.9, will have a physical thickness that can be considerably larger than a desired t_{eq}, while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a t_{eq} of 10 Å, not including any depletion/inversion layer effects. Thus, a reduced equivalent oxide thickness for transistors can be realized by using dielectric materials with higher dielectric constants than SiO_2.

The thinner equivalent oxide thickness required for lower transistor operating voltages and smaller transistor dimensions may be realized by a significant number of materials, but additional fabricating requirements makes determining a suitable replacement for SiO_2 difficult. The current view for the microelectronics industry is still for Si based devices. This requires that the gate dielectric employed be grown on a silicon substrate or silicon layer, which places significant constraints on the substitute dielectric material. During the formation of the dielectric on the silicon layer, there exists the possibility that a small layer of SiO_2 could be formed in addition to the desired dielectric. The result would effectively be a dielectric layer consisting of two sublayers in parallel with each other and the silicon layer on which the dielectric is formed. In such a case, the resulting capacitance would be that of two dielectrics in series. As a result, the t_{eq} of the dielectric layer would be the sum of the SiO_2 thickness and a multiplicative factor of the thickness, t, of the dielectric being formed, written as

$$t_{eq} = t_{SiO_2} + (\kappa_{ox} / \kappa)t.$$

Thus, if a SiO_2 layer is formed in the process, the t_{eq} is again limited by a SiO_2 layer. In the event that a barrier layer is formed between the silicon layer and the desired dielectric in which the barrier layer prevents the formation of a SiO_2 layer, the t_{eq} would be limited by the layer with the lowest dielectric constant.

However, whether a single dielectric layer with a high dielectric constant or a barrier layer with a higher dielectric constant than SiO_2 is employed, the layer interfacing with the silicon layer must provide a high quality interface to maintain a high channel carrier mobility.

One of the advantages using SiO_2 as a gate dielectric has been that the formation of the SiO_2 layer results in an amorphous gate dielectric. Having an amorphous structure for a gate dielectric provides for reducing problems of leakage current associated with grain boundaries in polycrystalline gate dielectrics that provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline gate dielectric can cause variations in the film's dielectric constant, along with uniformity and surface topography problems. Typically, materials having the advantage of a high dielectric constant relative to SiO_2 also have the disadvantage of a crystalline form, at least in a bulk configuration. The best candidates for replacing SiO_2 as a gate dielectric are those with high dielectric constant, which can be fabricated as a thin layer with an amorphous form.

High-κ materials include materials having a dielectric constant greater than silicon dioxide, for example, dielectrics materials having a dielectric constant greater than about twice the dielectric constant of silicon dioxide. Examples of such high-κ materials include Ta_2O_3, TiO_2, Al_2O_3, ZrO_2, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, and barium strontium titanate (BST). An appropriate high-κ gate dielectric to replace SiO_2 should have a large energy gap (E_g) and large energy barrier heights with Si for both electrons and holes. Generally, the bandgap is inversely related to the dielectric constant for a high-κ material, which lessens some advantages of the high-κ material. Dielectric layers of titanium aluminum oxide offer a material that can provide a relatively high dielectric constant with respect to silicon oxide and an acceptably high bandgap. The dielectric constant and bandgap for titanium aluminum oxide will range in value from that of Al_2O_3 to that of TiO_2. Al_2O_3 has a bandgap of about 8.7 eV and a dielectric constant of about 9, while TiO_2 has a bandgap of about 3.5 eV and a dielectric constant of about 80. Engineering a titanium aluminum oxide film can provide dielectric layers for electronic devices with dielectric constants of about 30 with bandgaps of about 4 eV.

Other characteristics for choosing a silicon oxide replacement include using materials that provide a sharp interface with silicon that may provide a low density of interface states, a large energy barrier from the conduction band to the Fermi level of the gate electrode to maintain leakage current at acceptable levels, and structural stability with contact electrodes and substrate material during device processing steps performed after providing the dielectric layer.

Embodiments for forming a titanium aluminum oxide film by atomic layer deposition may provide a film having a specific stoichiometry or it may be a non-stoichiometric titanium aluminum oxide. The expression $TiAlO_x$ is used herein to represent a stoichiometric and/or a non-stoichiometric titanium aluminum oxide. Embodiments of dielectric layers containing an atomic layer deposited titanium aluminum oxide layer have a larger dielectric constant than silicon dioxide. Such dielectric layers provide a significantly thinner equivalent oxide thickness compared with a silicon oxide layer having the same physical thickness. Alternately, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide thickness. This increased physical thickness aids in reducing leakage current.

Another consideration for selecting the material and method for forming a dielectric layer for use in electronic devices and systems concerns the roughness of a dielectric layer on a substrate. Surface roughness of the dielectric layer has a significant effect on the electrical properties of the gate oxide, and the resulting operating characteristics of the transistor. The leakage current through a physical 1.0 nm gate oxide increases by a factor of 10 for every 0.1 increase in the root-mean-square (RMS) roughness.

During a conventional sputtering deposition process stage, particles of the material to be deposited bombard the surface at a high energy. When a particle hits the surface, some particles adhere, and other particles cause damage. High energy impacts remove body region particles creating pits. The surface of such a deposited layer can have a rough contour due to the rough interface at the body region.

In an embodiment, a titanium aluminum oxide dielectric layer having a substantially smooth surface relative to other processing techniques is formed using atomic layer deposition (ALD). Further, forming such a dielectric layer

using atomic layer deposition can provide for controlling transitions between material layers. Thus, atomic layer deposited titanium aluminum oxide dielectric layers can have an engineered transition with a substrate surface.

ALD, also known as atomic layer epitaxy (ALE), is a modification of chemical vapor deposition (CVD) and is also called "alternatively pulsed-CVD." In ALD, gaseous precursors are introduced one at a time to the substrate surface mounted within a reaction chamber (or reactor). This introduction of the gaseous precursors takes the form of pulses of each gaseous precursor. In a pulse of a precursor gas, the precursor gas is made to flow into a specific area or region for a short period of time. Between the pulses, the reaction chamber is purged with a gas, which in many cases is an inert gas, and/or evacuated.

In a chemisorption-saturated ALD (CS-ALD) process, during the first pulsing phase, reaction with the substrate occurs with the precursor saturatively chemisorbed at the substrate surface. Subsequent pulsing with a purging gas removes precursor excess from the reaction chamber.

The second pulsing phase introduces another precursor on the substrate where the growth reaction of the desired film takes place. Subsequent to the film growth reaction, reaction byproducts and precursor excess are purged from the reaction chamber. With favourable precursor chemistry where the precursors adsorb and react with each other on the substrate aggressively, one ALD cycle can be preformed in less than one second in properly designed flow type reaction chambers. Typically, precursor pulse times range from about 0.5 sec to about 2 to 3 seconds.

In ALD, the saturation of all the reaction and purging phases makes the growth self-limiting. This self-limiting growth results in large area uniformity and conformality, which has important applications for such cases as planar substrates, deep trenches, and in the processing of porous silicon and high surface area silica and alumina powders. Significantly, ALD provides for controlling film thickness in a straightforward manner by controlling the number of growth cycles.

ALD was originally developed to manufacture luminescent and dielectric layers needed in electroluminescent displays. Significant efforts have been made to apply ALD to the growth of doped zinc sulfide and alkaline earth metal

sulfide films. Additionally, ALD has been studied for the growth of different epitaxial II-V and II-VI films, nonepitaxial crystalline or amorphous oxide and nitride films and multilayer structures of these. There also has been considerable interest towards the ALD growth of silicon and germanium films, but due to the difficult precursor chemistry, this has not been very successful.

The precursors used in an ALD process may be gaseous, liquid or solid. However, liquid or solid precursors should be volatile. The vapor pressure should be high enough for effective mass transportation. Also, solid and some liquid precursors may need to be heated inside the reaction chamber and introduced through heated tubes to the substrates. The necessary vapor pressure should be reached at a temperature below the substrate temperature to avoid the condensation of the precursors on the substrate. Due to the self-limiting growth mechanisms of ALD, relatively low vapor pressure solid precursors can be used though evaporation rates may somewhat vary during the process because of changes in their surface area.

There are several other characteristics for precursors used in ALD. The precursors should be thermally stable at the substrate temperature because their decomposition would destroy the surface control and accordingly the advantages of the ALD method that relies on the reaction of the precursor at the substrate surface. A slight decomposition, if slow compared to the ALD growth, can be tolerated.

The precursors should chemisorb on or react with the surface, though the interaction between the precursor and the surface as well as the mechanism for the adsorption is different for different precursors. The molecules at the substrate surface should react aggressively with the second precursor to form the desired solid film. Additionally, precursors should not react with the film to cause etching, and precursors should not dissolve in the film. Using highly reactive precursors in ALD contrasts with the selection of precursors for conventional CVD.

The by-products in the reaction should be gaseous in order to allow their easy removal from the reaction chamber. Further, the by-products should not react or adsorb on the surface.

In a reaction sequence ALD (RS-ALD) process, the self-limiting process sequence involves sequential surface chemical reactions. RS-ALD relies on chemistry between a reactive surface and a reactive molecular precursor. In an RS-ALD process, molecular precursors are pulsed into the ALD reaction chamber separately. The metal precursor reaction at the substrate is typically followed by an inert gas pulse to remove excess precursor and by-products from the reaction chamber prior to pulsing the next precursor of the fabrication sequence.

By RS-ALD, films can be layered in equal metered sequences that are all identical in chemical kinetics, deposition per cycle, composition, and thickness. RS-ALD sequences generally deposit less than a full layer per cycle. Typically, a deposition or growth rate of about 0.25 to about 2.00 Å per RS-ALD cycle can be realized.

The advantages of RS-ALD include continuity at an interface avoiding poorly defined nucleating regions that are typical for chemical vapor deposition (< 20 Å) and physical vapor deposition (< 50 Å), conformality over a variety of substrate topologies due to its layer-by-layer deposition technique, use of low temperature and mildly oxidizing processes, lack of dependence on the reaction chamber, growth thickness dependent solely on the number of cycles performed, and ability to engineer multilayer laminate films with resolution of one to two monolayers. RS-ALD processes allows for deposition control on the order on monolayers and the ability to deposit monolayers of amorphous films.

Herein, a sequence refers to the ALD material formation based on an ALD reaction of one precursor with its reactant precursor. For example, forming titanium oxide from a TiI_4 precursor and H_2O_2, as its reactant precursor, forms an embodiment of a titanium/oxygen sequence, which can also be referred to as titanium sequence. A cycle of a sequence includes pulsing a precursor, pulsing a purging gas for the precursor, pulsing a reactant precursor, and pulsing the reactant's purging gas. However, in forming a layer of a metal species, an ALD sequence deals with reacting a precursor containing the metal species with a substrate surface. A cycle for such a metal forming sequence includes pulsing a purging gas after pulsing the precursor containing the metal species. In an embodiment, a layer of titanium aluminum oxide is formed on a substrate

mounted in a reaction chamber using ALD in repetitive titanium and aluminum sequences using precursor gases individually pulsed into the reaction chamber. Alternately, solid or liquid precursors can be used in an appropriately designed reaction chamber.

Figure 1 shows an embodiment of an atomic layer deposition system 100 for processing a dielectric layer containing an insulating metal oxide film having multiple metal species, such as a titanium aluminum oxide film, constructed in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. The elements depicted permit discussion of the present invention such that those skilled in the art may practice the present invention without undue experimentation. In Figure 1, a substrate 110 is located inside a reaction chamber 120 of ALD system 100. Also located within the reaction chamber 120 is a heating element 130, which is thermally coupled to substrate 110 to control the substrate temperature. A gas-distribution fixture 140 introduces precursor gases to the substrate 110. Each precursor gas originates from individual gas sources 151-154 whose flow is controlled by mass-flow controllers 156-159, respectively. Gas sources 151-154 provide a precursor gas either by storing the precursor as a gas or by providing a location and apparatus for evaporating a solid or liquid material to form the selected precursor gas.

Also included in the ALD system are purging gas sources 161, 162, each of which is coupled to mass-flow controllers 166, 167, respectively. Furthermore, additional purging gas sources can be constructed in ALD system 100, one purging gas source for each precursor gas, for example. For a process that uses the same purging gas for multiple precursor gases less purging gas sources are required for ALD system 100. Gas sources 151-154 and purging gas sources 161-162 are coupled by their associated mass-flow controllers to a common gas line or conduit 170, which is coupled to the gas-distribution fixture 140 inside the reaction chamber 120. Gas conduit 170 is also coupled to vacuum pump, or exhaust pump, 181 by mass-flow controller 186 to remove excess precursor gases, purging gases, and by-product gases at the end of a purging sequence from the gas conduit.

Vacuum pump, or exhaust pump, 182 is coupled by mass-flow controller 187 to remove excess precursor gases, purging gases, and by-product gases at

the end of a purging sequence from reaction chamber 120. For convenience, control displays, mounting apparatus, temperature sensing devices, substrate maneuvering apparatus, and necessary electrical connections as are known to those skilled in the art are not shown in Figure 1. Though ALD system 100 is well suited for practicing the present invention, other ALD systems commercially available can be used.

The use, construction and fundamental operation of reaction chambers for deposition of films are understood by those of ordinary skill in the art of semiconductor fabrication. The present invention man be practiced on a variety of such reaction chambers without undue experimentation. Furthermore, one of ordinary skill in the art will comprehend the necessary detection, measurement, and control techniques in the art of semiconductor fabrication upon reading the disclosure.

The elements of ALD system 100 can be controlled by a computer. To focus on the use of ALD system 100 in the various embodiments of the present invention, the computer is not shown. Those skilled in the art can appreciate that the individual elements such as pressure control, temperature control, and gas flow within ALD system 100 can be under computer control.

In an embodiment, a method for forming a dielectric layer includes forming an insulating metal oxide having multiple metal species. The method of forming the insulating metal oxide includes forming a first layer of a first metal and/or a second metal by atomic layer deposition. In an embodiment, the first layer is formed having a thickness that is at most substantially two monolayers. In an embodiment, the first layer may be formed having one of the multiple metals with the remaining one or more metals incorporated into the first layer on subsequent processing. In an embodiment, a first layer formed with one metal species may have a thickness ranging from one to two monolayers.

After forming the first layer of metal, the first layer is annealed using oxygen. The oxygen may be substantially atomic oxygen, substantially molecular oxygen, or may include atomic oxygen and molecular oxygen. With one metal species formed as a thin first layer, deposition of the other metals to form the desired insulating metal oxide may be concluded by atomic layer deposition following the annealing to form the initial first layer as a first layer of

the desired insulating metal oxide. Such a subsequently formed metal oxide having multiple metal species may be further annealed using oxygen.

After annealing the first layer, a second layer of an insulating metal oxide having the multiple metal species is formed onto the first layer by atomic layer deposition to form a contiguous layer. The second layer of insulating metal oxide may be formed in a manner similar to forming and annealing the first layer. In an embodiment, the second layer of insulating metal oxide containing multiple metal species is constructed by forming a number of layers by atomic layer deposition with a number of oxygen annealings between atomic layer deposition cycles and between layer formation. The completed annealed first layer and second layer provides one contiguous insulating metal oxide having multiple metal species. In an embodiment, the insulating metal oxide is a titanium aluminum oxide film.

Figure 2 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film. At 210, titanium and/or aluminum are deposited onto a substrate surface by atomic layer deposition to form a first layer. The first layer may be formed to provide uniform coverage of the desired area of the substrate surface for forming the dielectric layer to avoid forming a silicon oxide in an interface between the substrate surface and the dielectric layer. A number of precursors containing titanium may be used to deposit the titanium and a number of precursors containing aluminum may be used to deposit the aluminum. In an embodiment, titanium is deposited before aluminum. In an embodiment, aluminum is deposited before titanium. Alternately, titanium and aluminum may be jointly deposited using precursors that substantially do no react with each other, but react at the substrate surface. In an embodiment, one of either titanium or aluminum may be deposited by atomic layer deposition with the other metal deposited at a later stage of the process for forming the titanium aluminum oxide film. In embodiment, the deposited titanium and/or aluminum form one or more monolayers over the desired area of the substrate surface for forming the dielectric layer. In embodiment, titanium is deposited over a portion of the desired area of the substrate surface for forming the dielectric layer with aluminum deposited over the remaining portion of the desired area. Such partial

coverage can be realized by pulsing a titanium precursor for a pulsing period that provides the partial coverage of a monolayer on the surface and then pulsing an aluminum precursor provides uniform formation of a monolayer over the surface including the surface having deposited titanium. Alternately, the aluminum precursor may be pulsed prior to the titanium precursor.

At 220, the first layer is annealed using oxygen. In an embodiment, oxygen annealing is conducted after depositing one of titanium and aluminum and again after depositing the other one of titanium and aluminum. Such oxygen annealing following individual deposition of aluminum and titanium may be conducted after forming a monolayer of each metal. In an embodiment, the oxygen used is atomic oxygen. In an embodiment, the oxygen used is molecular oxygen. Alternately, the oxygen includes a combination of atomic and molecular oxygen. The annealing of the first layer provides for forming the first layer as a titanium aluminum oxide layer in which an interface, between the first layer and the substrate surface on which it is deposited, is substantially without a silicon oxide layer or has a silicon oxide layer having a thickness of at most two monolayers. In other embodiments, a silicon oxide layer having a thickness of at most four monolayers is formed in the interface. Titanium and aluminum have oxide formation energies that are more negative than silicon, and as a result, the formation of the first layer having titanium and/or aluminum on the surface with a silicon substrate will reduce the likelihood for formation of interfacial silicon oxide. Using atomic oxygen may provide lower leakage current than using molecular oxygen. Using atomic oxygen may also provide a smaller amount of interfacial silicon oxide than using molecular oxygen. In an embodiment, after annealing a deposited layer of one of either titanium or aluminum, metal atoms of either titanium or aluminum not deposited before annealing are deposited to form the first layer as a $TiAlO_x$ layer.

At 230, after annealing the first layer, a second layer of titanium aluminum oxide is formed onto the first layer by atomic layer deposition to form a contiguous titanium aluminum oxide layer. The second layer may be formed in a similar deposition and annealing manner as the first layer. Alternately, the second layer may be formed as multiple contiguous $TiAlO_x$ layers, each layer formed in a manner similar to forming the first $TiAlO_x$ layer. In an embodiment,

the second titanium aluminum oxide layer is formed by atomic layer deposition using a titanium/oxide sequence and an aluminum/oxide sequence. Alternately, the second layer may be formed as multiple contiguous $TiAlO_x$ layers, each layer formed by atomic layer deposition using a titanium/oxide sequence and an aluminum/oxide sequence with an oxygen annealing conducted in between forming each layer. In an embodiment, the second titanium aluminum oxide layer may be formed as multiple contiguous layers having a number of oxygen annealings performed between selected ALD cycles or between selected layers. Further, a multi-layered process for the second TiAlOx layer may have a number of layers formed in a manner similar to the first layer and a number of layers formed using a selected permutation of titanium/oxide and an aluminum/oxide ALD sequences. After forming the titanium aluminum film, other dielectric layers such as nitride layers and/or insulating metal oxide layers may be formed as part of the dielectric layer. The dielectric layer may be formed as a nanolaminate. An embodiment of a nanolaminate may include a layer of titanium oxide and the titanium aluminum oxide film. Alternately, the dielectric layer may be formed substantially as the titanium aluminum oxide film.

In various embodiments, the structure of the interface between the dielectric layer and the substrate on which it is disposed is controlled to limit the inclusion of silicon oxide, since a silicon oxide layer would reduce the effective dielectric constant of the dielectric layer. The material composition and its properties for an interface layer are typically dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate interface layer, a silicon oxide interface layer or other composition interface layer, may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

Figure 3 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film. At 310, a layer of titanium aluminum oxide is formed by atomic layer deposition to provide a first layer. The $TiAlO_x$ layer may be formed using a number of cycles having various permutations of titanium/oxide sequences and aluminum/oxide

sequences. A number of titanium containing precursors and a number of oxygen containing precursors may be used in the titanium sequences. A number of aluminum containing precursors and a number of oxygen containing precursors may be used in the aluminum sequences. In an embodiment, the initial ALD sequence is conducted with a pulsing period sufficient to provide metal, aluminum or titanium, coverage uniformly over the desired area of the substrate surface on which the dielectric is being formed. In an embodiment, the initial ALD sequence is a combination of titanium and aluminum sequences conducted with a pulsing period sufficient to provide aluminum and titanium coverage uniformly over the desired area of the substrate surface on which the dielectric is being formed. In an embodiment, the combination sequence does not use titanium precursors and aluminum precursors that interact with each other but react with the substrate surface to deposit titanium and aluminum.

At 320, the first layer of titanium aluminum is annealed using oxygen. In an embodiment, annealing is conducted with the first layer formed as a monolayer. In an embodiment, annealing is conducted with the first layer formed as at most five monolayers. Oxygen annealing may be conducted for thin layers of the first layer to aid in the formation of the $TiAlO_x$ first layer maintaining an interface with the substrate surface that has a silicon oxide interfacial layer of at most four monolayers. In an embodiment, the interface may be formed substantially without interfacial silicon oxide. In an embodiment, the annealing oxygen is essentially atomic oxygen. In an embodiment, the annealing oxygen is essentially molecular oxygen. Alternately, the annealing oxygen includes a combination of atomic and molecular oxygen. Using atomic oxygen may provide lower leakage current than using molecular oxygen. Using atomic oxygen may also provide a smaller amount of interfacial silicon oxide than using molecular oxygen.

At 330, after annealing the first layer, a second layer of titanium aluminum oxide is formed onto the first layer by atomic layer deposition to form a contiguous titanium aluminum oxide layer. The second layer may be formed in a similar deposition and annealing manner as the first layer, at 310 and 320. Alternately, the second layer may be formed as multiple contiguous $TiAlO_x$ layers, each layer formed in a manner similar to forming the first $TiAlO_x$ layer.

Alternately, the second layer may be formed as multiple contiguous $TiAlO_x$ layers, each layer formed by atomic layer deposition using a titanium/oxide sequence and an aluminum/oxide sequence with an oxygen annealing conducted in between forming each layer. In an embodiment, the second titanium aluminum oxide layer may be formed as multiple contiguous layers having a number of oxygen annealings performed between selected ALD cycles or between selected layers. Further, a multi-layered process for the second TiOx layer may have a number of layers formed using a selected permutation of titanium/oxide and an aluminum/oxide ALD sequences. After forming the titanium aluminum film, other dielectric layers such as nitride layers and/or insulating metal oxide layers may be formed as part of the dielectric layer. The dielectric layer may be formed as a nanolaminate. An embodiment of a nanolaminate may include a layer of titanium oxide and the titanium aluminum oxide film. Alternately, the dielectric layer may be formed substantially as the titanium aluminum oxide film.

In the various embodiments, the thickness of $TiAlO_x$ film is related to the number of ALD cycles performed for each metal species and the growth rate associated with the selected permutations of sequences in the cycles. As can be understood by those skilled in the art, particular effective growth rates for the engineered $TiAlO_x$ film can be determined during normal initial testing of the ALD system for processing a titanium aluminum oxide dielectric for a given application without undue experimentation.

Atomic layer deposition of the individual components of the titanium aluminum oxide layer allows for individual control of each precursor pulsed into the reaction chamber. Thus, each precursor is pulsed into the reaction chamber for a predetermined period, where the predetermined period can be set separately for each precursor. Additionally, for various embodiments for ALD formation of a titanium aluminum oxide layer, each precursor can be pulsed into the reaction under separate environmental conditions. The substrate can be maintained at a selected temperature and the reaction chamber maintained at a selected pressure independently for pulsing each precursor. Appropriate temperatures and pressures may be maintained, whether the precursor is a single precursor or a mixture of precursors. During atomic layer deposition, the

pulsing of the precursor gases is separated by purging the reaction chamber with a purging gas following each pulsing of a precursor. In an embodiment, nitrogen gas is used as the purging gas following the pulsing of each precursor used in a cycle to form a film of titanium aluminum oxide. Additionally, the reaction chamber can also be purged by evacuating the reaction chamber.

Figure 4 illustrates a flow diagram of elements for an embodiment of a method to form a dielectric layer containing a titanium aluminum oxide film using atomic layer deposition. This embodiment can be implemented with the atomic layer deposition system 100 of Figure 1. At 410, a substrate 110 is prepared. The substrate used for forming a integrated circuit is typically a silicon or silicon containing material. In other embodiments, germanium, gallium arsenide, silicon-on-sapphire substrates, or other suitable substrates may be used. This preparation process includes cleaning substrate 110 and forming layers and regions of the substrate, such as drains and sources of a metal oxide semiconductor (MOS) transistor, prior to forming a gate dielectric. Alternately, these active regions may be formed after forming the dielectric layer, depending on the over-all fabrication process implemented. In an embodiment, the substrate is cleaned to provide an initial substrate depleted of its native oxide. In an embodiment, the initial substrate is cleaned to also provide a hydrogen-terminated surface. In an embodiment, a silicon substrate undergoes a final hydrofluoric (HF) rinse prior to ALD processing to provide the silicon substrate with a hydrogen-terminated surface without a native silicon oxide layer.

Cleaning immediately preceding atomic layer deposition aids in reducing an occurrence of silicon oxide as an interface between a silicon based substrate and a dielectric formed using the atomic layer deposition process. The material composition and its properties of an interface layer are typically dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate interface layer, a SiO_2 interface layer or other composition interface layer, may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

The sequencing of the formation of the regions of the transistor being processed follows typical sequencing that is generally performed in the fabrication of a MOS transistor as is well known to those skilled in the art. Included in the processing prior to forming a gate dielectric is the masking of substrate regions to be protected during the gate dielectric formation, as is typically performed in MOS fabrication. In this embodiment, the unmasked region includes a body region of a transistor, however one skilled in the art will recognize that other semiconductor device structures may utilize this process. Additionally, the substrate 110 in its ready for processing form is conveyed into a position in reaction chamber 120 for ALD processing.

At 415, a titanium precursor is pulsed into reaction chamber 120. In an embodiment, TiI_4 is used as a precursor. The TiI_4 is pulsed into reaction chamber 120 through the gas-distribution fixture 140 onto substrate 110. The flow of the TiI_4 is controlled by mass-flow controller 156 from gas source 151. In embodiment, the substrate temperature is maintained between about 300 °C and about 400 °C by heating element 130 for a TiI_4 precursor. In another embodiment, a $TiCl_4$ precursor is used with the substrate temperature maintained between about 425 °C and about 600 °C. Other titanium precursors may be used. The titanium precursor reacts with the surface of the substrate 110 in the desired region defined by the unmasked areas of the substrate 110. In various embodiments, the presence of residual chlorine in a titanium aluminum oxide dielectric layer may be reduced or eliminated providing a substantially chlorine free film by using metal precursors other than metal chlorides in the ALD processing of each metal, titanium and aluminum. Use of a metal iodine as a precursor results in a film substantially free of residual iodine. As a result, metal halide precursors other than chloride metal precursors may be used. Eliminating residual chloride in such dielectric layers may provide reduced leakage current for devices having these dielectric layers.

At 420, a first purging gas is pulsed into the reaction chamber 120. In an embodiment, nitrogen is used as a purging gas and a carrier gas. The nitrogen flow is controlled by mass-flow controller 166 from the purging gas source 161 into the gas conduit 170. Using the pure nitrogen purge avoids overlap of the

precursor pulses and possible gas phase reactions. Following the purge, a first reactant precursor is pulsed into the reaction chamber 120, at 425.

For the titanium sequence using TiI_4 as the precursor, oxygen precursor, H_2O_2, may be used as the reactant precursor. For a titanium sequence using $TiCl_4$ as the precursor, oxygen precursor, H_2O, may be used as the reactant precursor. The reactant precursor is pulsed into the reaction chamber 120 through gas conduit 170 from gas source 152 by mass-flow controller 157. The reactant precursor aggressively reacts at the surface of substrate 110.

Following the pulsing of a first reactant precursor, a second purging gas is injected into the reaction chamber 120, at 430. Nitrogen gas is used to purge the reaction chamber after pulsing each precursor gas in a titanium/oxygen sequence. Excess precursor gas, and reaction by-products are removed from the system by the purge gas in conjunction with the exhausting of the reaction chamber 120 using vacuum pump 182 through mass-flow controller 187, and exhausting of the gas conduit 170 by the vacuum pump 181 through mass-flow controller 186.

At 435, an aluminum precursor is pulsed into reaction chamber 120. In an embodiment, the aluminum precursor is trimethyl aluminum. Other aluminum precursors may be used. In an embodiment, the substrate temperature is maintained between about 300 °C and a pressure of about 1 Torr. Mass-flow controller 158 regulates the pulsing of the aluminum precursor to the surface of the substrate 110 through gas-distribution fixture 140 from gas source 153.

At 440, a third purging gas is introduced into the system. Nitrogen gas can also be used as a purging and carrier gas. The nitrogen flow is controlled by mass-flow controller 167 from the purging gas source 162 into the gas conduit 170 and subsequently into the reaction chamber 120. In another embodiment, argon gas is used as the purging gas. Following the pulsing of the third purging gas, a second reactant precursor is pulsed into the reaction chamber 120, at 445. The reactant precursor is selected to produce an oxidizing reaction for the aluminum at the substrate surface. In an embodiment, the reactant precursor is H_2O vapor. Mass-flow controller 159 regulates the water vapor pulsing into reaction chamber 120 through gas conduit 170 from gas source 154. The H_2O vapor aggressively reacts at the surface of substrate 110.

Following the pulsing of the second reactant precursor, a fourth purging gas is injected into reaction chamber 120, at 450. Nitrogen gas may be used to purge the reaction chamber after pulsing each precursor gas in the aluminum/oxygen sequence. In another embodiment, argon gas may be used as the purging gas. Excess precursor gas, and reaction by-products are removed from the system by the purge gas in conjunction with the exhausting of reaction chamber 120 using vacuum pump 182 through mass-flow controller 187, and exhausting of the gas conduit 170 by the vacuum pump 181 through mass-flow controller 186.

At 455, titanium sequences and aluminum sequences are repeated for a number of cycles to form a first layer of titanium aluminum oxide. In an embodiment, the number of cycles is selected to provide a first layer of titanium aluminum oxide having a thickness of about one to two monolayers. In an embodiment, the number of cycles is selected to provide a first layer of titanium aluminum oxide having a thickness of at most four monolayers. In an embodiment, a titanium/aluminum cycle may include permutations of a number of titanium sequences with a number of aluminum sequences.

At 460, the titanium aluminum layer is annealed using oxygen. The annealing may be conducted at 500 ° C. The annealing may be conducted as a room temperature exposure to oxygen. In an embodiment, the annealing oxygen is substantially atomic oxygen. In another embodiment, the annealing oxygen is substantially molecular oxygen. Alternately, the annealing oxygen includes atomic oxygen and molecular oxygen.

At 465, titanium sequences and aluminum sequences are repeated for a number of cycles to form a second titanium aluminum oxide layer onto the first layer of titanium aluminum oxide. The two layers form a contiguous titanium aluminum oxide layer.

At 470, determination is made as to whether the desired thickness for the titanium aluminum oxide film has been formed. The desired thickness is related to the number of ALD cycles to form the sublayers of the titanium aluminum oxide film. If the number of completed cycles is less than the number needed to form the desired thickness for the titanium aluminum oxide film, additional ALD processing is conducted. Prior to performing additional ALD processing, a

determination is made, at 375, as to whether additional annealing is desired. If additional annealing is desired, the process continues at 460. In various embodiments, a number of oxygen annealing procedures may be implemented between the ALD cycles. If no additional annealing is desired, the process continues at 465.

The thickness of a titanium aluminum oxide film is determined by a fixed growth rate for the pulsing periods and precursors used, set at a value such as N nm/ combined cycle, dependent upon the number of cycles of the aluminum sequence relative to the titanium sequence that form a combined sequence. For a desired titanium aluminum oxide film thickness, t, in an application such as forming a gate dielectric of a MOS transistor, the ALD process is repeated for t/N total combined cycles. Once the t/N cycles have completed, no further ALD processing for titanium aluminum oxide is required.

At 480, after forming the desired thickness for the titanium aluminum oxide film, the process continues with completing device fabrication. Further processing of the device may include annealing a device structure that includes the dielectric layer. Such annealing may aid in reducing leakage current through the dielectric layer containing the titanium aluminum film. The titanium aluminum oxide film processed at these relatively low temperatures may provide an amorphous dielectric layer. In an embodiment, completing the device includes completing the formation of a transistor. In another embodiment, completing the device includes completing the formation of a capacitor. Alternately, completing the process includes completing the construction of a memory device having an array with access transistors formed with gate dielectrics containing atomic layer deposited titanium aluminum oxide. Further, in another embodiment, completing the process includes the formation of an electronic system including an information handling device that uses electronic devices with transistors formed with dielectric layers containing atomic layer deposited titanium aluminum oxide. Typically, information handling devices such as computers include many memory devices, having many access transistors.

It can appreciated by those skilled in the art that the elements of a method for forming an atomic layer deposited titanium aluminum oxide film in the

embodiment of Figure 4 can be performed with various number of titanium sequences relative to the number of aluminum sequences. In selecting the number of titanium sequences and aluminum sequences relative to each other, a titanium aluminum oxide film can be engineering with bandgap and dielectric constant characteristics ranging from that of Al_2O_3 to that of TiO_2. In another embodiment, the ALD processing of a titanium aluminum oxide dielectric layer may provide a dielectric layer having a dielectric constant of about 30. In various embodiments, a dielectric layer of titanium aluminum oxide is provided such that a interface between the dielectric layer and a substrate surface on which it is disposed has substantially no silicon oxide layer or a silicon oxide layer of at most two monolayers thickness. The selection of the dielectric constant may be conducted in a optimization, or trade-off, process with improving the current leakage characteristics of the film.

The embodiments described herein provide a process for growing a dielectric layer having a wide range of useful equivalent oxide thickness, t_{eq}, associated with a dielectric constant in the range from about 9 to about 80. The lower end of this range is associated with a titanium aluminum oxide film that is aluminum rich. For example, an aluminum rich film but may viewed as an aluminum oxide film doped with titanium. The upper end of the range for a titanium aluminum film is associated with a titanium aluminum oxide film that is titanium rich. For example, an titanium rich film but may viewed as a titanium oxide film doped with aluminum. For a titanium aluminum film with the amount of titanium and aluminum in approximately equal proportions, the dielectric constant is about 30. A dielectric constant of about 30 provides for a t_{eq} that is about 13% of a given silicon dioxide thickness. In an embodiment, a dielectric layer containing a atomic layer deposited titanium aluminum oxide film has a t_{eq} that is less than 10 Å. In an embodiment, a dielectric layer containing a atomic layer deposited titanium aluminum oxide film has a t_{eq} that is less than 3 Å. Alternately, for an acceptable silicon dioxide thickness, an embodiment for a titanium aluminum oxide with a dielectric constant of about 30 may be about seven to eight times larger than the acceptable silicon dioxide thickness providing enhanced probability for reducing leakage current. Further, dielectric layers of titanium aluminum oxide formed in various embodiments

may provide not only thin t_{eq} films, but also amorphous films with relatively low leakage current. Additionally, the novel process can be implemented to form transistors, capacitors, memory devices, and other electronic systems including information handling devices.

A transistor 500 as depicted in Figure 5 may be constructed by forming a source region 520 and a drain region 530 in a silicon based substrate 510 where source and drain regions 520, 530 are separated by a body region 532. Body region 532 defines a channel having a channel length 534. A dielectric layer is disposed on substrate 510. A gate 550 is formed over and contacts gate dielectric 540. The dielectric layer contains an insulating metal oxide having multiple metal species formed by atomic layer deposition in multiple layers with one or more oxygen annealings between atomic layer deposition cycles. The metal oxide structure may be formed as a contiguous metal oxide film. In an embodiment, the insulating metal oxide is a titanium aluminum oxide film. The dielectric is formed on substrate 510. The resulting dielectric layer forms gate dielectric 540. Gate dielectric 540 may be realized as a dielectric layer formed substantially of a titanium aluminum oxide film. Gate dielectric 540 may be dielectric layer containing one or more layers of dielectric material in which at least one layer is titanium aluminum oxide film.

An interfacial layer 533 may form between body region 532 and gate dielectric 540. In an embodiment, interfacial layer 533 may be limited to a relatively small thickness compared to gate dielectric 540, or to a thickness significantly less than gate dielectric 540 as to be effectively eliminated. In an embodiment, interfacial layer 533 is configured such that it is substantially without a silicon oxide layer. In an embodiment, interfacial layer 533 includes a silicon oxide layer having a thickness of at most four monolayers. In an embodiment, interfacial layer 533 includes a silicon oxide layer having a thickness of at most two monolayers. Forming the substrate, gate, and the source and drain regions may be performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor may be conducted with standard fabrication processes, also as known to those skilled in the art. In an embodiment, gate dielectric 540 may be realized as a gate insulator in a silicon CMOS transistor.

Use of such a gate dielectric including an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

Figure 6 shows an embodiment of a configuration of a floating gate transistor 600 having an insulating metal oxide having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. The metal oxide structure may be formed as a contiguous metal oxide film. In an embodiment, the insulating metal oxide is a titanium aluminum oxide film. Transistor 600 includes a silicon based substrate 610 with a source 620 and a drain 630 separated by a body region 632. Body region 632 between source 620 and drain 630 defines a channel region having a channel length 634. Located above body region 632 is a stack 655 including a gate dielectric 640, a floating gate 652, a floating gate dielectric 642, and a control gate 650. In an embodiment, floating gate 652 is formed over and contacts gate dielectric 640. An interfacial layer 633 may form between body region 632 and gate dielectric 640. In an embodiment, interfacial layer 633 may be limited to a relatively small thickness compared to gate dielectric 640, or to a thickness significantly less than gate dielectric 640 as to be effectively eliminated. In an embodiment, interfacial layer 633 is configured such that it is substantially without a silicon oxide layer. In an embodiment, interfacial layer 633 includes a silicon oxide layer having a thickness of at most four monolayers. In an embodiment, interfacial layer 633 includes a silicon oxide layer having a thickness of at most two monolayers.

Gate dielectric 640 includes a dielectric containing an atomic layer deposited insulating metal oxide formed in embodiments similar to those described herein. In an embodiment, the metal oxide is a titanium aluminum oxide film. Gate dielectric 640 may be realized as a dielectric layer formed substantially of titanium aluminum oxide. Gate dielectric 640 may include multiple layers in which at least one layer is substantially titanium aluminum oxide. In an embodiment, gate dielectric 640 may include multiple layers where a substantially titanium aluminum oxide contacts body region 632.

In an embodiment, floating gate dielectric 642 includes a dielectric layer having an atomic layer deposited insulating metal oxide formed in embodiments similar to those described herein. Floating gate dielectric 642 may be realized as a dielectric layer formed substantially of titanium aluminum oxide. Floating gate dielectric 642 may include multiple layers in which at least one layer is substantially titanium aluminum oxide. In an embodiment, control gate 650 is formed over and contacts floating gate dielectric 642.

Alternately, both gate dielectric 640 and floating gate dielectric 642 may be formed as dielectric layers including an insulating metal oxide having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. The metal oxide structure may be formed as a contiguous metal oxide film. In an embodiment, the insulating metal oxide is a titanium aluminum oxide film. Gate dielectric 640, and floating gate dielectric 642 may be realized by embodiments similar to those described herein with the remaining elements of the transistor 600 formed using processes known to those skilled in the art.

In an embodiment, gate dielectric 640 forms a tunnel gate insulator and floating gate dielectric 642 forms an inter-gate insulator in flash memory devices, where gate dielectric 640 and/or floating gate dielectric 642 include an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. In an embodiment, gate dielectric 640 and floating gate dielectric 642 include atomic layer deposited titanium aluminum oxide. Use of dielectric layers configured in various embodiments is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

The embodiments of methods for forming dielectric layers containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles may also be applied to forming capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment for forming a capacitor 700 illustrated in Figure 7, a method includes forming a first conductive layer 710, forming a dielectric layer

720 containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition on first conductive layer 710, and forming a second conductive layer 730 on dielectric layer 720. The insulating metal oxide may be a titanium aluminum oxide film. Dielectric layer 720 including an insulating metal oxide film having multiple metal species may be formed using any of the embodiments described herein.

An interfacial layer 715 may form between first conductive layer 710 and dielectric layer 720. In an embodiment, interfacial layer 715 may be limited to a relatively small thickness compared to dielectric layer 720, or to a thickness significantly less than dielectric layer 720 as to be effectively eliminated. In an embodiment, interfacial layer 715 is configured such that it is substantially without a silicon oxide layer. In an embodiment, interfacial layer 715 includes a silicon oxide layer having a thickness of at most four monolayers. In an embodiment, interfacial layer 715 includes a silicon oxide layer having a thickness of at most two monolayers.

Dielectric layer 720 may be realized as a dielectric layer formed substantially of titanium aluminum oxide. Dielectric layer 720 may include multiple layers in which at least one layer is substantially titanium aluminum oxide. In an embodiment, dielectric layer 720 may include multiple layers where a substantially titanium aluminum oxide film contacts first conductive layer 710. Embodiments for dielectric layer 720 in a capacitor includes, but is not limited to, dielectrics in DRAM capacitors and dielectrics in capacitors in analog, radio frequency (RF), and mixed signal integrated circuits.

Various embodiments for a dielectric film containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles may provide for enhanced device performance by providing devices with reduced leakage current. In an embodiment, such improvements in leakage current characteristics may be attained by forming one or more layers of an atomic layer deposited titanium aluminum oxide in a nanolaminate structure with other dielectric layers including other metal oxides such as titanium oxide. The transition from one layer of the nanolaminate to another layer of the nanolaminate provides further disruption to a tendency for an ordered structure

in the nanolaminate stack. The term "nanolaminate" means a composite film of ultra thin layers of two or more materials in a layered stack, where the layers are alternating layers of materials of the composite film. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range. Further, each individual material layer of the nanolaminate can have a thickness as low as a monolayer of the material or as high as 20 nanometers. In an embodiment, a $TiO_x/TiAlO_x$ nanolaminate contains alternating layers of a titanium oxide and a titanium aluminum oxide.

Figure 8 depicts a nanolaminate structure 800 for an embodiment of a dielectric structure including an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles. In an embodiment, the metal oxide is a titanium aluminum oxide. In an embodiment, nanolaminate structure 800 includes a plurality of layers 805-1, 805-2 to 805-N, where at least one layer contains a titanium aluminum oxide film formed according to an embodiment herein. The other layers may be other dielectric layers or dielectric metal oxides. The sequencing of the layers depends on the application. In an embodiment, an atomic layer deposited titanium aluminum oxide film is the first layer formed on a substrate. In an embodiment, nanolaminate structure 800 contains an atomic layer deposited titanium aluminum oxide film in contact with conductive contact 810 and/or conductive contact 820. The effective dielectric constant associated with nanolaminate structure 800 is that attributable to N capacitors in series, where each capacitor has a thickness defined by the thickness of the corresponding layer. By selecting each thickness and the composition of each layer, a nanolaminate structure can be engineered to have a predetermined dielectric constant. Embodiments for structures such as nanolaminate structure 800 may be used as nanolaminate dielectrics in NROM flash memory devices as well as other integrated circuits.

Transistors, capacitors, and other devices having dielectric films containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles formed by the methods described above may be implemented into memory devices and electronic

systems including information handling devices. Embodiments of these information handling devices may include wireless systems, telecommunication systems, and computers. Further, embodiments of electronic devices having dielectric films containing an insulating metal oxide film having multiple metal species, such as a titanium aluminum oxide film, may be realized as integrated circuits.

Figure 9 illustrates a diagram for an electronic system 900 having one or more devices having a dielectric layer containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles fabricated according to various embodiments. In an embodiment, such a dielectric layer includes a titanium aluminum oxide film. Electronic system 900 includes a controller 905, a bus 915, and an electronic device 925, where bus 915 provides electrical conductivity between controller 905 and electronic device 925. In various embodiments, controller 905 and/or electronic device 925 include an embodiment for a dielectric layer an insulating metal oxide film having multiple metal species formed by atomic layer deposition as previously discussed herein. Electronic system 900 may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

Figure 10 depicts a diagram of an embodiment of a system 1000 having a controller 1005 and a memory 1025. Controller 1005 and/or memory 1025 may include a dielectric layer having an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles fabricated according to various embodiments of the present invention. In an embodiment, such a dielectric layer includes a titanium aluminum oxide film. System 1000 also includes an electronic apparatus 1035, and a bus 1015, where bus 1015 provides electrical conductivity between controller 1005 and electronic apparatus 1035, and between controller 1005 and memory 1025. Bus 1015 may include an address, a data bus, and a control bus, each independently configured. Alternately, bus 1015 may use common conductive lines for providing address,

data, and/or control, the use of which is regulated by controller 1005. In an embodiment, electronic apparatus 1035 may be additional memory configured similar as memory 1025. An embodiment may include an additional peripheral device or devices 1045 coupled to bus 1015. In an embodiment, controller 1005 is a processor. Any of controller 1005, memory 1025, bus 1015, electronic apparatus 1035, and peripheral device devices 1045 may include a dielectric layer including an insulating metal oxide film having multiple metal species formed according to various embodiments of the present invention. In an embodiment, such a dielectric layer includes a titanium aluminum oxide film. System 1000 may include, but is not limited to, information handling devices, telecommunication systems, and computers.

Peripheral devices 1045 may include displays, additional storage memory, or other control devices that may operate in conjunction with controller 1005. Alternately, peripheral devices 1045 may include displays, additional storage memory, or other control devices that may operate in conjunction with controller 1005 and/or memory 1025.

Memory 1025 may be realized as a memory device containing a dielectric layer including an insulating metal oxide film having multiple metal species formed according to various embodiments of the present invention. In an embodiment, such a dielectric layer includes a titanium aluminum oxide film. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging DRAM technologies. .

Formation of dielectric layers containing an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles, processed in relatively low temperatures, may be amorphous and possess smooth surfaces. In an embodiment, such a dielectric layer includes

a titanium aluminum oxide film. Such titanium aluminum oxide films can provide enhanced electrical properties due to their smoother surface resulting in reduced leakage current. Additionally, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide thickness, where the increased thickness would also reduce leakage current. These properties of embodiments of dielectric layers allow for application as dielectric layers in numerous electronic devices and systems.

Capacitors, transistors, higher level ICs or devices including memory devices, and electronic systems are constructed utilizing the novel process for forming a dielectric film having an ultra thin equivalent oxide thickness, t_{eq}. Gate dielectric layers or films including an insulating metal oxide film having multiple metal species formed by atomic layer deposition in a multiple layer process with one or more oxygen annealings between atomic layer deposition cycles are formed having a dielectric constant (κ) substantially higher than that of silicon oxide. These dielectric films are capable of a t_{eq} thinner than SiO_2 gate dielectrics of the same physical thickness. Alternately, the high dielectric constant relative to silicon dioxide allows the use of much larger physical thickness of these high-κ dielectric materials for the same t_{eq} of SiO_2. Forming the relatively larger thickness aids in processing gate dielectrics and other dielectric layers in electronic devices and systems.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of embodiments of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon studying the above description. The scope of the present invention includes any other applications in which embodiment of the above structures and fabrication methods are used. The scope of the embodiments of the present

invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method comprising:

forming a dielectric layer containing an insulating metal oxide in an integrated circuit, the forming of the insulating metal oxide including:

forming a first layer by atomic layer deposition, the first layer having one or more metals from a group of a first metal and a second metal;

annealing the first layer using oxygen; and

forming, after annealing the first layer, a second layer of an insulating metal oxide of the one or more metals onto the first layer by atomic layer deposition to form a contiguous layer.

2. The method of claim 1, wherein annealing the first layer using oxygen includes annealing the first layer substantially using atomic oxygen.

3. The method of claim 1, wherein forming a first layer includes forming the first layer as a layer of the first metal and the second metal.

4. The method of claim 1, wherein forming a first layer includes forming the first layer having a thickness of about one monolayer.

5. The method of claim 1, wherein forming a first layer includes forming the first layer having a thickness of at most substantially two monolayers.

6. The method of claim 1, wherein forming a second layer of an insulating metal oxide includes:

depositing the one or more metals on the first layer by atomic layer deposition; and

annealing the deposited one or more metals using oxygen.

7. The method of claim 1, wherein forming a dielectric layer containing an insulating metal oxide includes forming a dielectric layer containing a titanium

aluminum oxide film, forming a first layer includes forming a layer having one or more metals from a group of titanium and aluminum, and forming a second layer includes forming a layer of titanium aluminum oxide.

8. The method of claim 7, wherein annealing the first layer using oxygen includes annealing the first layer substantially using atomic oxygen.

9. The method of claim 7, wherein forming a layer having one or more metals includes forming the first layer as a layer of titanium and aluminum.

10. The method of claim 7, wherein forming a second layer of titanium aluminum oxide includes:

depositing one or more metals from a group of titanium and aluminum on the first layer by atomic layer deposition; and

annealing the deposited one or more metals using oxygen.

11. The method of claim 7, wherein forming the first layer and annealing the first layer includes:

depositing titanium by atomic layer deposition;

annealing the deposited titanium using oxygen;

depositing aluminum by atomic layer deposition after annealing the deposited titanium; and

annealing the deposited aluminum using oxygen to form the first layer into a layer of titanium aluminum oxide.

12. The method of claim 7, wherein forming the first layer and annealing the first layer includes:

depositing aluminum by atomic layer deposition;

annealing the deposited aluminum using oxygen;

depositing titanium by atomic layer deposition after annealing the deposited aluminum; and

annealing the deposited titanium using oxygen to form the first layer into a layer of titanium aluminum oxide.

13. The method of claim 7, wherein forming a dielectric layer includes forming a nanolaminate of titanium oxide and the titanium aluminum oxide film.

14. The method of claim 7, wherein the method includes forming an integrated circuit and forming the dielectric layer as a gate insulator in a transistor in the integrated circuit.

15. The method of claim 7, wherein forming the dielectric layer includes forming the dielectric layer to contact a substrate on which it is disposed substantially by a combination of titanium and aluminum atoms.

16. The method of claim 1, wherein forming a dielectric layer containing an insulating metal oxide includes forming a dielectric layer containing a titanium aluminum oxide film, the forming of the titanium aluminum oxide film including:

forming the first layer as a layer of titanium aluminum oxide by atomic layer deposition;

annealing the first layer using atomic oxygen; and

forming the second layer as a layer of titanium aluminum oxide.

17. The method of claim 16, wherein forming the first layer includes forming the first layer as a monolayer of titanium aluminum oxide.

18. The method of claim 16, wherein forming the layer of titanium aluminum oxide includes using TiI_4 as a precursor.

19. The method of claim 16, wherein forming the second layer of titanium aluminum oxide includes using $TiCl_4$ as a precursor.

20. The method of claim 16, wherein forming the layer of titanium aluminum oxide includes using trimethyl aluminum as a precursor.

21. The method of claim 16, wherein forming a dielectric layer includes forming a nanolaminate of titanium oxide and the titanium aluminum oxide film.

22. The method of claim 16, wherein the method includes forming the integrated circuit and forming the dielectric layer as a gate insulator in a transistor in the integrated circuit.

23. The method of claim 16, wherein the method includes forming the integrated circuit and forming the dielectric layer as a gate insulator in a CMOS transistor in the integrated circuit.

24. The method of claim 16, wherein forming the dielectric layer includes forming the dielectric layer to contact a substrate on which it is disposed is substantially provided by a combination of titanium and aluminum atoms.

25. The method of claim 1, wherein the method includes:

forming a memory array in which the dielectric layer is disposed including:

forming the dielectric layer as a dielectric layer containing a titanium aluminum oxide film, the forming of the titanium aluminum oxide film including:

forming the first layer as a layer having one or more metals from a group of titanium and aluminum by atomic layer deposition;

annealing the first layer using atomic oxygen; and

forming the second layer as a layer of titanium aluminum oxide; and

forming an address decoder, the address decoder coupled to the memory array.

26. The method of claim 25, wherein forming the first layer includes forming the first layer as a layer of titanium and aluminum.

27. The method of claim 25, wherein forming the second layer of titanium aluminum oxide includes:

depositing the one or more metals on the first layer by atomic layer deposition; and

annealing the deposited one or more metals using atomic oxygen.

28. The method of claim 25, wherein forming the first layer and annealing the first layer includes:

depositing titanium by atomic layer deposition;

annealing the deposited titanium using atomic oxygen;

depositing aluminum by atomic layer deposition after annealing the deposited titanium; and

annealing the deposited aluminum using atomic oxygen to form the first layer into a layer of titanium aluminum oxide.

29. The method of claim 25, wherein forming the first layer and annealing the first layer includes:

depositing aluminum by atomic layer deposition;

annealing the deposited aluminum using atomic oxygen;

depositing titanium by atomic layer deposition after annealing the deposited aluminum; and

annealing the deposited titanium using atomic oxygen to form the first layer into a layer of titanium aluminum oxide.

30. The method of claim 25, wherein the method includes forming a memory device and forming the dielectric layer as a gate insulator of a transistor in the memory array.

31. The method of claim 25, wherein the method includes forming a flash memory device and forming the dielectric layer as an inter-gate insulator between and contacting a floating gate and a control gate of a transistor in the flash memory device.

32. The method of claim 1, wherein the method includes:

forming a memory array in which the dielectric layer is disposed including:

forming the dielectric layer as a dielectric layer containing a titanium aluminum oxide film, the forming of the titanium aluminum oxide film including:

forming the first layer as a layer of titanium aluminum oxide by atomic layer deposition;

annealing the first layer using oxygen; and

forming the second layer as a layer of titanium aluminum oxide; and

forming an address decoder coupled to the memory array.

33. The method of claim 32, wherein annealing the first layer using oxygen includes annealing the first layer substantially using atomic oxygen.

34. The method of claim 32, wherein forming the first layer as a layer of titanium aluminum oxide includes using a number of cycles to form at most four monolayers of titanium aluminum oxide as the first layer.

35. The method of claim 32, wherein forming the dielectric layer includes forming a silicon oxide interface layer between and contacting the dielectric layer and a substrate on which the dielectric is disposed such that the silicon oxide interface layer is at most two monolayers thick.

36. The method of claim 32, wherein forming a dielectric layer includes forming the dielectric layer substantially without a silicon oxide interface layer between and contacting the dielectric layer and a substrate on which the dielectric is disposed.

37. The method of claim 32, wherein forming the dielectric layer includes forming the dielectric layer substantially as the titanium aluminum oxide film.

38. The method of claim 32, wherein forming the dielectric layer includes forming the dielectric layer such that contact to a substrate on which the dielectric layer is disposed is substantially provided by titanium atoms, aluminum atoms, or a combination of titanium and aluminum atoms.

39. The method of claim 32, wherein the method includes forming a memory device and forming the dielectric layer as a gate insulator of a transistor in the memory array.

40. The method of claim 32, wherein the method includes forming a flash memory device and forming the dielectric layer as an inter-gate insulator between and contacting a floating gate and a control gate of a transistor in the flash memory device.

41. The method of claim 32, wherein the method includes forming a memory device including forming the dielectric layer as a dielectric of a capacitor in the memory device.

42. A method comprising:

providing a controller;

coupling an integrated circuit to the controller, wherein the integrated circuit includes a dielectric layer formed according to the method of claim 1 with the dielectric layer containing the insulating metal oxide formed as a dielectric layer containing a titanium aluminum oxide film, wherein forming the titanium aluminum oxide film includes:

forming the first layer as a layer of titanium aluminum oxide by atomic layer deposition; and

forming the second layer as a layer of titanium aluminum oxide.

43. The method of claim 42, wherein coupling an integrated circuit to the controller includes coupling a memory device formed as the integrated circuit having the dielectric layer containing the titanium aluminum oxide film.

44. The method of claim 42, wherein providing a controller includes providing a processor.

45. The method of claim 42, wherein coupling an integrated circuit to the controller includes coupling a mixed signal integrated circuit formed as the integrated circuit having the dielectric layer containing the titanium aluminum oxide film.

46. The method of claim 42, wherein forming the first layer as a layer of titanium aluminum oxide includes using a titanium halide precursor.

47. The method of claim 42, wherein forming a dielectric layer includes forming a silicon oxide interface layer between the dielectric layer and a substrate on which the dielectric layer is formed such that the silicon oxide interface layer is at most two monolayers thick.

48. The method of claim 42, wherein forming a dielectric layer includes forming the dielectric layer substantially without a silicon oxide interface layer between the dielectric layer and a substrate on which the dielectric layer is formed.

49. The method of claim 42, wherein forming a dielectric layer includes forming the dielectric layer to contact a substrate on which the dielectric layer is formed substantially by titanium atoms, aluminum atoms, or a combination of titanium and aluminum atoms.

50. The method of claim 42, wherein the method includes forming an information handling system.

51. The method of claim 42, wherein forming an information handling system includes forming a computer.

52. The method of claim 42, wherein forming an information handling system includes forming a wireless communication system.

53. An electronic device comprising:

a substrate having an integrated circuit; and

a dielectric layer containing an atomic layer deposited titanium aluminum oxide film disposed on the substrate as part of the integrated circuit such that an interface between and contacting the dielectric layer and the substrate includes at most two monolayers of thickness.

54. The electronic device of claim 53, wherein the dielectric layer includes a silicon oxide interface layer such that the silicon oxide interface layer is at most two monolayers thick.

55. The electronic device of claim 53, wherein the interface is substantially without a silicon oxide interface layer.

56. The electronic device of claim 53, wherein the dielectric layer is substantially the atomic layer deposited titanium aluminum oxide film.

57. The electronic device of claim 53, wherein the interface is substantially provided by titanium atoms, aluminum atoms, or a combination of titanium and aluminum atoms.

58. The electronic device of claim 53, wherein the electronic device includes a transistor in the integrated circuit, the transistor having the dielectric layer as a gate insulator in the transistor.

59. The electronic device of claim 53, wherein the electronic device includes a CMOS transistor in the integrated circuit, the CMOS transistor having the dielectric layer as a gate insulator.

60. The electronic device of claim 53, wherein the electronic device includes a capacitor having the dielectric layer as a dielectric between two electrodes in the capacitor.

61. The electronic device of claim 53, wherein the dielectric layer is a nanolaminate that includes an insulating metal oxide layer and the atomic layer deposited titanium aluminum oxide film.

62. An electronic device comprising:

a substrate having an integrated circuit; and

a dielectric layer containing an atomic layer deposited titanium aluminum oxide film disposed on the substrate as part of the integrated circuit, the atomic layer deposited titanium aluminum oxide film formed by the method of claim 16.

63. The electronic device of claim 62, wherein an interface between the dielectric layer and a substrate on which the dielectric layer is disposed is substantially without a silicon oxide layer.

64. The electronic device of claim 62, wherein the dielectric layer is substantially the atomic layer deposited titanium aluminum oxide film.

65. The electronic device of claim 62, wherein an interface between the dielectric layer and a substrate on which the dielectric layer is disposed is substantially provided by titanium atoms, aluminum atoms, or a combination of titanium and aluminum atoms.

66. The electronic device of claim 62, wherein the electronic device is a memory.

67. A system comprising:

a controller; and

the electronic device of claim 62.

68. The system of claim 67, wherein an interface between the dielectric layer and the substrate on which the dielectric layer is disposed is substantially without a silicon oxide interface layer.

69. The system of claim 67, wherein an interface between the dielectric layer and the substrate on which the dielectric layer is disposed is substantially provided by titanium atoms, aluminum atoms, or a combination of titanium and aluminum atoms.

70. A memory comprising:

a memory array, the memory array including the electronic device of claim 53; and

an address decoder in the substrate, the address decoder coupled to the memory array.

71. The memory of claim 70, wherein the interface includes a silicon oxide interface layer having at most two monolayers of thickness.

72. The memory of claim 70, wherein the interface is substantially without a silicon oxide interface layer with the substrate.

73. The memory of claim 70, wherein the memory is an electronic device including a processor.

74. The memory of claim 70, wherein the memory is a memory device and the dielectric layer is a gate insulator of a transistor in the memory array.

75. The memory of claim 70, wherein the memory is a flash memory device.

76. The memory of claim 75, wherein the dielectric layer is an inter-gate insulator between and contacting a floating gate and a control gate of a transistor in the flash memory device.

77. The memory of claim 75, wherein the dielectric layer is a gate insulator between and contacting a floating gate and a channel of a transistor in the flash memory device.

78. The memory of claim 70, wherein the dielectric layer is a dielectric of a capacitor in the memory.

79. A system comprising:

a controller; and

the electronic device of claim 53 configured in the integrated circuit, the integrated circuit coupled to the controller.

80. The system of claim 79, wherein the interface includes a silicon oxide interface layer at most two monolayers thick.

81. The system of claim 79, wherein the interface is substantially without a silicon oxide interface layer.

82. The system of claim 79, wherein the integrated circuit includes a memory.

83. The system of claim 79, wherein the controller includes a processor.

84. The system of claim 79, wherein the integrated circuit includes a mixed signal integrated circuit.

85. The system of claim 79, wherein the system is an information handling system.

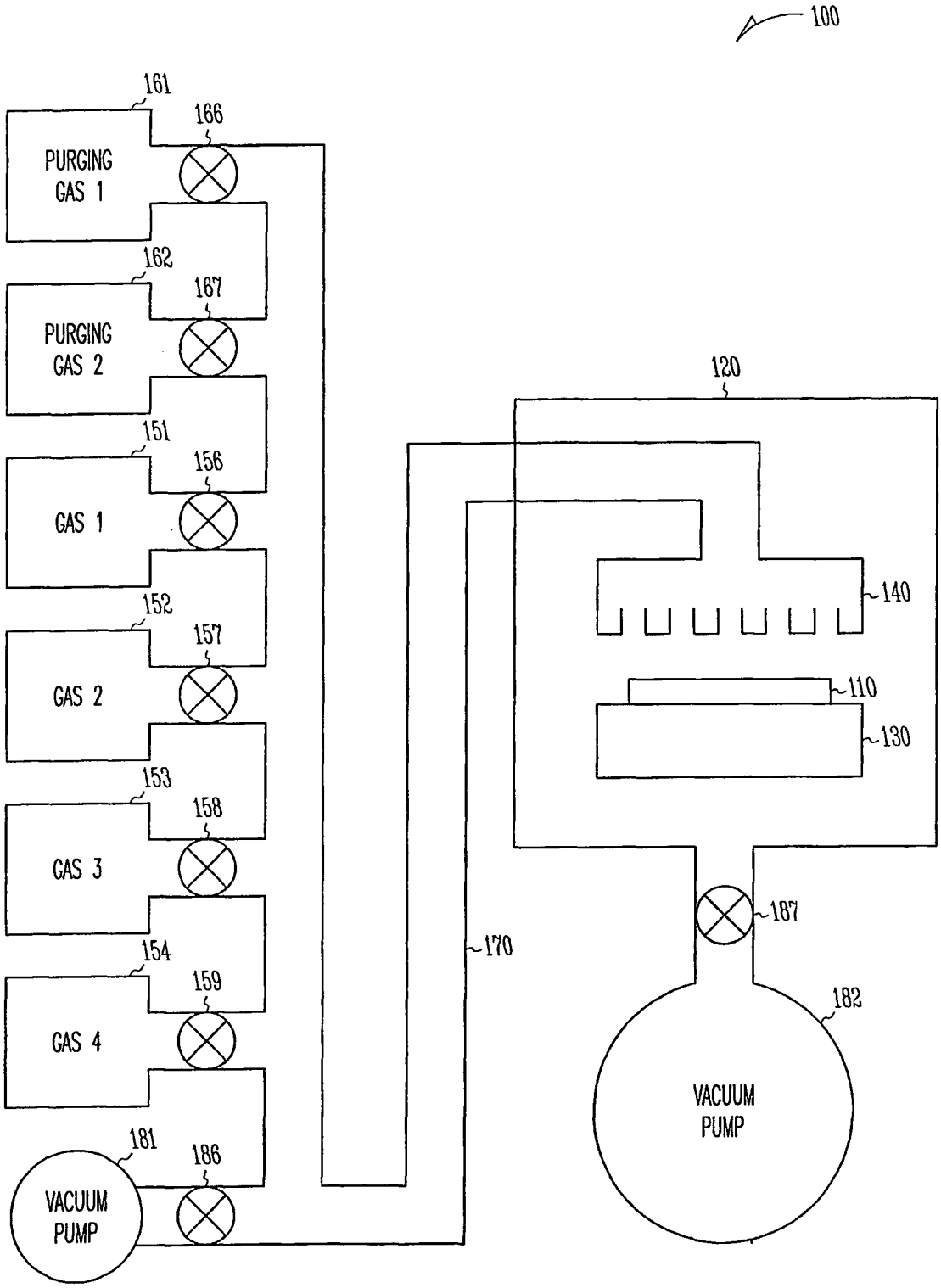

100
161
166
PURGING GAS 1
162
167
PURGING GAS 2
151
156
GAS 1
152
157
GAS 2
153
158
GAS 3
154
159
GAS 4
181
186
VACUUM PUMP
120
140
110
130
187
170
182
VACUUM PUMP

FIG. 1

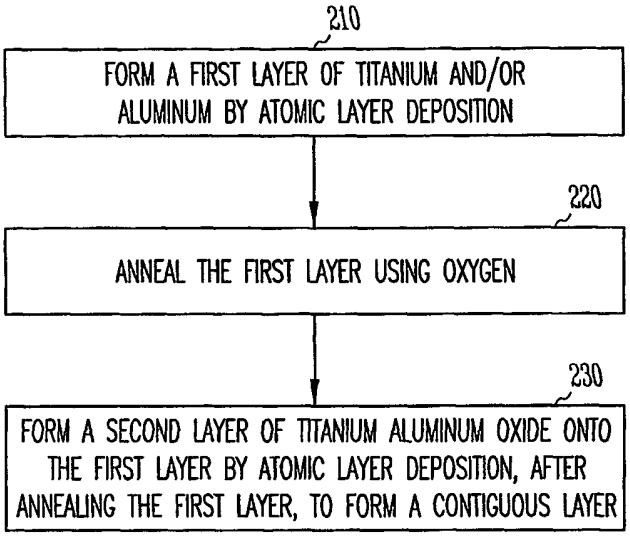

210
FORM A FIRST LAYER OF TITANIUM AND/OR ALUMINUM BY ATOMIC LAYER DEPOSITION
220
ANNEAL THE FIRST LAYER USING OXYGEN
230
FORM A SECOND LAYER OF TITANIUM ALUMINUM OXIDE ONTO THE FIRST LAYER BY ATOMIC LAYER DEPOSITION, AFTER ANNEALING THE FIRST LAYER, TO FORM A CONTIGUOUS LAYER

FIG. 2

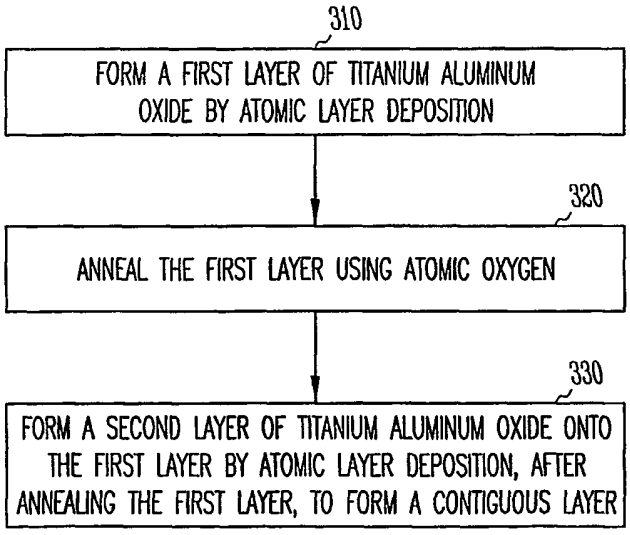

310
FORM A FIRST LAYER OF TITANIUM ALUMINUM OXIDE BY ATOMIC LAYER DEPOSITION
320
ANNEAL THE FIRST LAYER USING ATOMIC OXYGEN
330
FORM A SECOND LAYER OF TITANIUM ALUMINUM OXIDE ONTO THE FIRST LAYER BY ATOMIC LAYER DEPOSITION, AFTER ANNEALING THE FIRST LAYER, TO FORM A CONTIGUOUS LAYER

FIG. 3

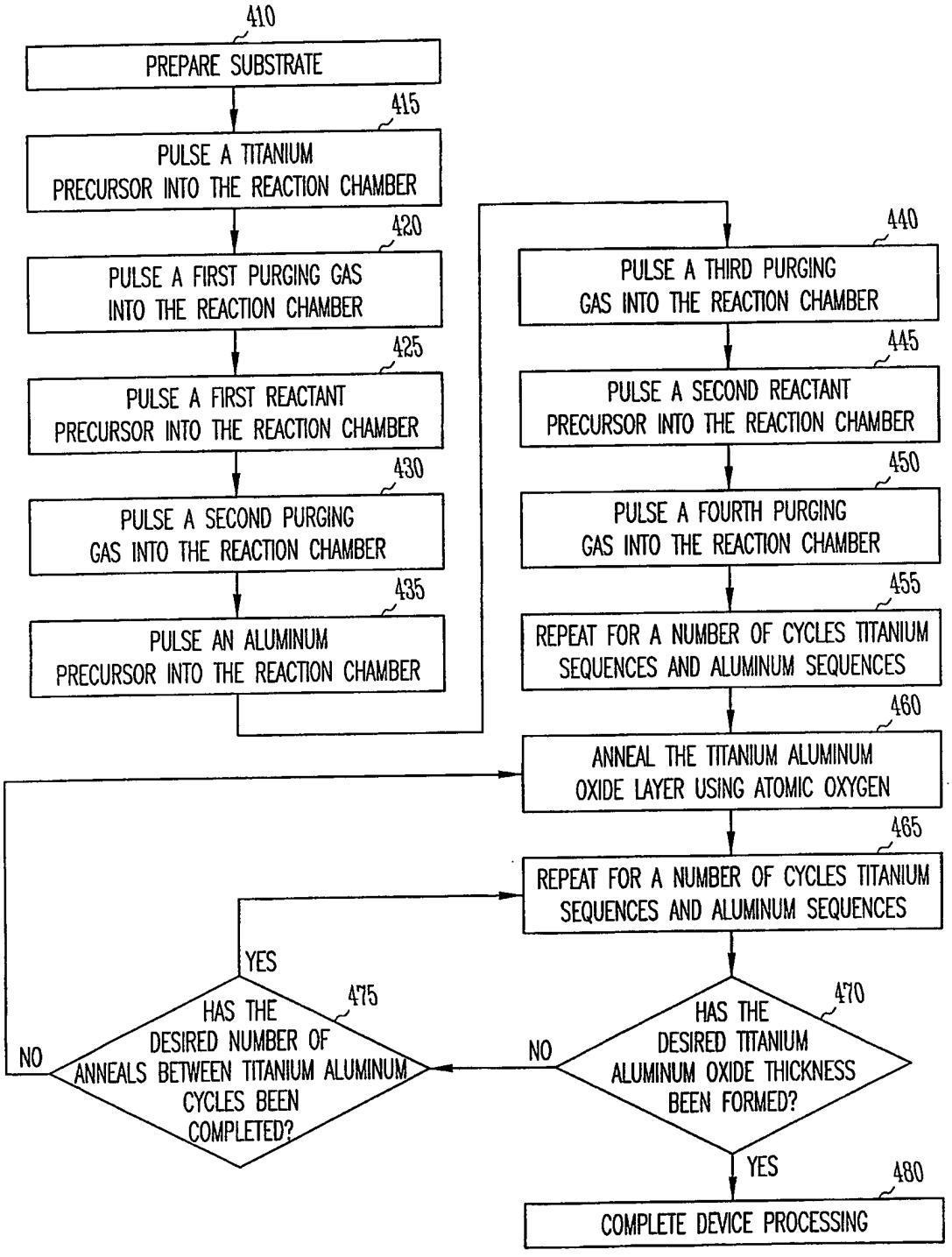

410
PREPARE SUBSTRATE
415
PULSE A TITANIUM PRECURSOR INTO THE REACTION CHAMBER
420
PULSE A FIRST PURGING GAS INTO THE REACTION CHAMBER
425
PULSE A FIRST REACTANT PRECURSOR INTO THE REACTION CHAMBER
430
PULSE A SECOND PURGING GAS INTO THE REACTION CHAMBER
435
PULSE AN ALUMINUM PRECURSOR INTO THE REACTION CHAMBER
440
PULSE A THIRD PURGING GAS INTO THE REACTION CHAMBER
445
PULSE A SECOND REACTANT PRECURSOR INTO THE REACTION CHAMBER
450
PULSE A FOURTH PURGING GAS INTO THE REACTION CHAMBER
455
REPEAT FOR A NUMBER OF CYCLES TITANIUM SEQUENCES AND ALUMINUM SEQUENCES
460
ANNEAL THE TITANIUM ALUMINUM OXIDE LAYER USING ATOMIC OXYGEN
465
REPEAT FOR A NUMBER OF CYCLES TITANIUM SEQUENCES AND ALUMINUM SEQUENCES
470
HAS THE DESIRED TITANIUM ALUMINUM OXIDE THICKNESS BEEN FORMED?
NO
YES
475
HAS THE DESIRED NUMBER OF ANNEALS BETWEEN TITANIUM ALUMINUM CYCLES BEEN COMPLETED?
NO
YES
480
COMPLETE DEVICE PROCESSING

FIG. 4

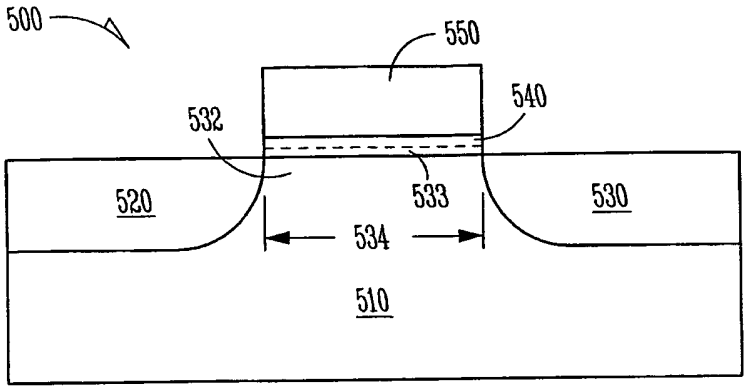

500
550
540
532
533
520
530
534
510

FIG. 5

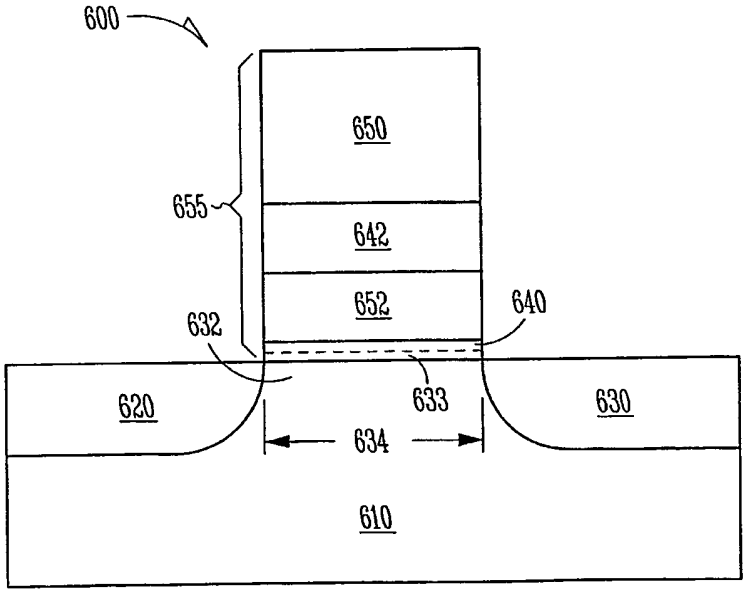

600
650
655
642
652
640
632
633
620
630
634
610

FIG. 6

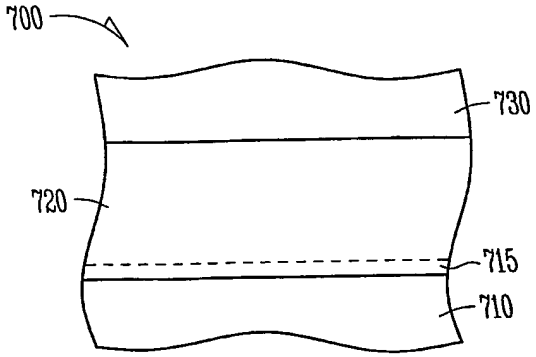


FIG. 7

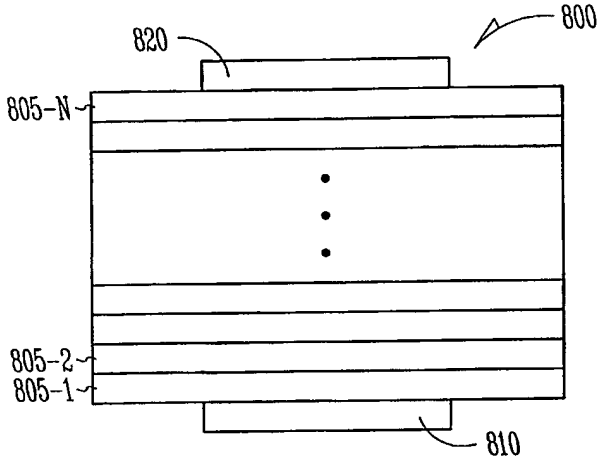


FIG. 8

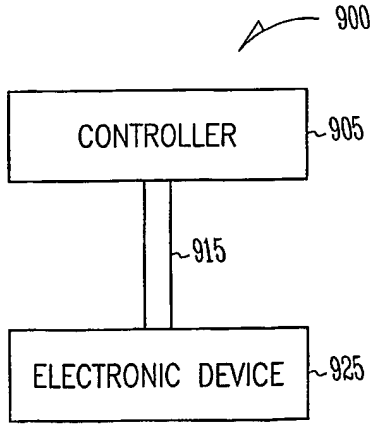


FIG. 9

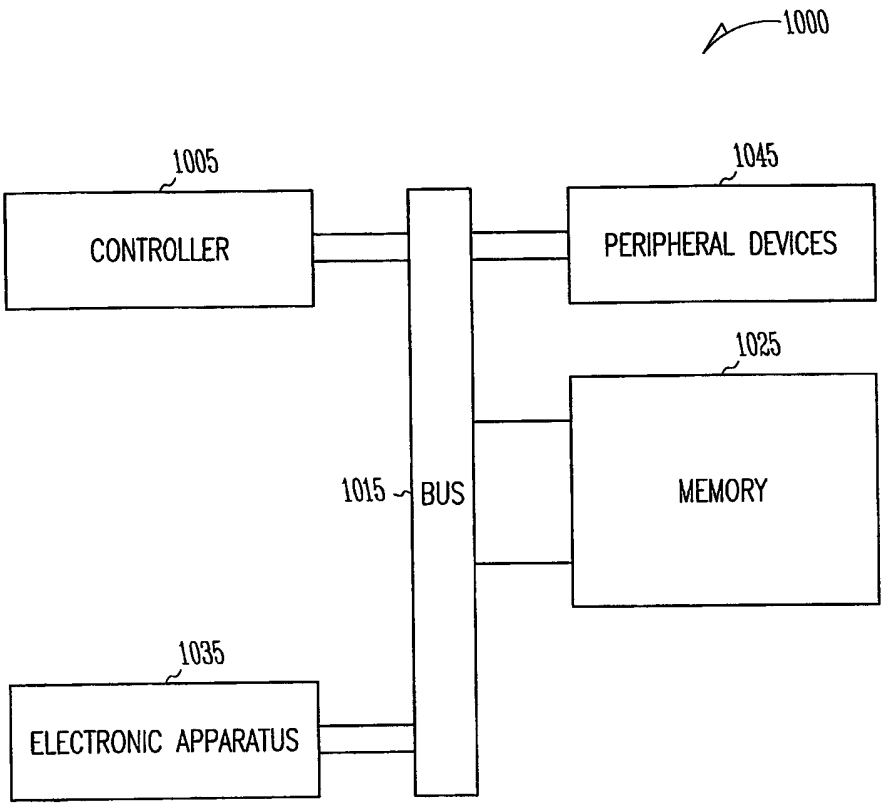

1000
1005
CONTROLLER
1045
PERIPHERAL DEVICES
1025
MEMORY
1015
BUS
1035
ELECTRONIC APPARATUS

FIG. 10

INTERNATIONAL SEARCH REPORT

ational Application No
/US2005/031159

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/314 H01L21/28 C23C16/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, CHEM ABS Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2003/003635 A1 (PARANJPE AJIT P ET AL) 2 January 2003 (2003-01-02) paragraph '0005! - paragraph '0034!; claims 1-3 -----	1,2 3-52
X	RITALA M ET AL: "ATOMIC LAYER DEPOSITION OF OXIDE THIN FILMS WITH METAL ALKOXIDES AS OXYGEN SOURCES" SCIENCE, AMERICAN ASSOCIATION FOR THE ADVANCEMENT OF SCIENCE,, US, vol. 288, no. 5464, 14 April 2000 (2000-04-14), pages 319-321, XP001147249 ISSN: 0036-8075	53-85
Y	page 319 - page 320; table 1 -----	3-52
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 January 2006	24/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bakker, J

INTERNATIONAL SEARCH REPORT

itional Application No
/US2005/031159

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	K. IWAMOTO ET AL.: "Advanced layer-by-layer deposition and annealing process for high-quality high-k dielectrics formation" ELECTROCHEMICAL SOCIETY PROC. (ADVANCED SHORT-TIME THERMAL PROCESSING FOR SI-BASED CMOS DEVICES), vol. 2003, no. 14, 2003, pages 265-272, XP008058238	1
A	page 265 - page 267; figure 1	2-52
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Y	US 2004/110391 A1 (AHN KIE Y ET AL) 10 June 2004 (2004-06-10) paragraph '0052! - paragraph '0053!	11,12,19
X	US 2003/181060 A1 (ASAI MASAYUKI ET AL) 25 September 2003 (2003-09-25)	53
A	paragraph '0119! - paragraph '0184!	11,12
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A	US 2004/161899 A1 (LUO TIEN YING ET AL) 19 August 2004 (2004-08-19) claims 1,2	2,8,27, 33

INTERNATIONAL SEARCH REPORT

Information on patent family members

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/US2005/031159

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